request in the communication area in a pre-defined record format and the first processor schedules and completes the request via a USB host controller.

5. (Amended) The USB host system of Claim 1 where the main processor interfaces the host system via a standard microprocessor bus.

7. (Amended) The USB host system of Claim 1 where data in the communication area is directly sent out on a USB bus.

9. (Amended) The USB host system of Claim 1 where the USB host system provides a USB function to the main processor.

10. (Amended) The USB host system of Claim 1 where the USB host system is used to provide a USB host function to the said second processor which runs an operating system supporting USB , by intercepting call to a USB driver in the operating system.

11. (Amended) A USB host system operationally coupled to a computing system, comprising:

a first processor implementing a function for managing a USB host controller with or without an operating system running on the computing system;

a down stream USB port;

an interface between the first processor and a second processor that provides a high-level USB pipe view of a USB system to an application program running on the second processor in the computing system.

24. (Amended) A USB host comprising:

a first processor implementing a function of a USB system;

a downstream USB port; and

a memory accessible by the first processor and a second processor external to the USB host, where a first area of the memory with first predetermined format is used for a first type of

transfer, and a second area of the memory with a second predetermined format is used for a second type of transfer.

46. (Amended) The USB host of Claim 41 where the second processor runs an operating system that supports USB and USB transfer request by the said second processor to USB driver on the second processor on the second processor is carried out by the USB host.

49. A USB host system operationally coupled to a computing system with a main processor, comprising:

a processor that interfaces with the main processor via a communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the processor schedules and completes the request via a USB host controller.

50. The USB host system of Claim 49, wherein the processor returns status and data to the main processor based on a request from the main processor.

51. The USB host system of Claim 49, wherein the communication area is a dual port memory with plural registers.

52. The USB host system of Claim 49, wherein the main processor may poll the communication area and/or be notified by an interrupt generated by the processor.

53. The USB system of Claim 49, wherein the communication area is divided into a first area with a predefined format for a first type of transfer, and a second area with a second pre-defined format for a second type of transfer.

54. The USB host system of Claim 49, wherein the main processor and the processor are operationally coupled via a standard microprocessor bus interface.